REMARKS

This is a full and timely response to the Final Office Action mailed by the U.S. Patent and Trademark Office on September 13, 2007. Claims 1-11 and 13-18 remain pending in the present application. Claim 12 has been canceled. Claims 1, 7 and 13 are amended. The subject matter of amended claims 1, 7 and 13 is supported in at least paragraph 22 and FIG. 2B of Applicant's original specification. Accordingly, no new matter is introduced.

In view of the foregoing amendments and following remarks, reconsideration and allowance of the present application and claims are respectfully requested.

I. Claim Rejection Under 35 USC § 102(b) – Claim 7

A. Statement of the Rejection

Claim 7 stands rejected under 35 USC § 102(b) as allegedly being anticipated by U.S. Patent No.: 5,189,705 to Lavaud, hereafter *Lavaud*.

B. Discussion of the Rejections

It is axiomatic that "[a]nticipation requires the disclosure in a single cited art reference of *each element* of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983)(*Emphasis added.*). "The element must be arranged as required by the claims." *In re Bond,* 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Therefore, every claimed feature of the claimed invention must be represented and arranged as required in the claims for the applied reference to constitute a proper rejection under 35 U.S.C. § 102.

Applicant has amended independent claim 7 to include at least one feature that is not disclosed, taught or suggested by *Lavaud*.

Applicant's claim 7, as amended, is directed to a method of generating a modulated square-wave audio signal that includes the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem." *Lavaud* fails to disclose, teach, or suggest at least Applicant's claimed method step.

In contrast with Applicant's claimed method, FIG. 2 of *Lavaud* shows a circuit arrangement for adjusting the volume of a signal in an audio system. The instantaneous volume level is tested constantly to determine whether it is equal to or higher than a previously-stored threshold. Further increase in volume is inhibited after the threshold has been attained, so that the current volume level is retained independent of actuation of volume controls. By actuating a switch, the volume may be further increased even after the threshold has been exceeded. *See, Abstract Lavaud.*

Thus, *Lavaud* discloses a circuit and method for setting a maximum controlled volume threshold for users unaware of the override switch (T2). That is, volume control inputs are accepted and applied via the counter to the digital-to-analog converter until the stored threshold is less than the counter value. When this is the case, the output of comparator is inverted and applied at AND gate G1, which prevents the train of pulses from being forwarded to the counter.

The circuit and method disclosed by *Lavaud* does not apply a modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem. In contrast with Applicant's claimed method, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier. In accordance with column 2, lines 10-14, the signal emitted by the counter is forwarded by a bus line B to a digital-to-analog converter, the analog-output voltage of which is used to control an amplifier. In accordance with column 2, lines 21-23, when an H level is emitted from the comparator, AND gate G1 prevents additional pulses, I, from reaching the counter. Accordingly, the counter state remains steady (i.e., the signal on bus B is constant) and cannot be increased, even when the incremental generator (volume control) is activated.

In contrast with *Lavaud*, which applies a steady-state counter value to the digital-to-analog converter when the comparator output indicates that the volume control threshold has been exceeded, Applicant's claimed method includes the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem." *Lavaud* does not disclose, teach, or suggest Applicant's claimed method step.

FIG. 2 of *Lavaud* shows that the output of the comparator is used to control the flow of pulses, I, from the encoder to the counter. As described above, when the threshold volume control input level is exceeded, pulses are not received at the counter. Accordingly, the counter output value remains fixed until the override switch (T2) is closed or the volume control input level falls below the threshold value. A fixed counter value (the only input to the amplifier and loudspeaker shown in *Lavaud*) does not anticipate Applicant's method, which includes the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem."

Accordingly, each feature of the claimed method is not disclosed in *Lavaud*. Consequently, independent claim 7, as amended, is allowable over *Lavaud* and the rejection of claim 7 should be withdrawn.

II. Claim Rejections Under 35 USC § 103 – Claims 1-6, 8-10 and 13 - 18

A. Statement of the Rejections

Claims 1 and 6 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud* in view of U.S. Patent No. 5,165,017 to Eddington *et al.* (*Eddington*).

Claim 2 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud* and *Eddington*, as applied to claim 1, in further view of U.S. Patent No. 3,932,849 to Welch (*Welch*).

Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud* and *Eddington*, as applied to claim 1, in further view of U.S. Patent No. 4,724,493 to Nakamura (*Nakamura*).

Claim 5 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud* and *Eddington*, as applied to claim 1, in further view of U.S. Patent Application Publication No. 20020048193 to Tanikawa *et al.* (*Tanikawa*).

Claim 8 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud*, as applied to claim 7, in further view of *Welch*.

Claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud*, as applied to claim 7, in further view of *Nakamura*.

Claims 13 and 18 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud* in view of *Eddington* in further view of Applicant's Admitted Prior Art (*AAPA*).

Claim 14 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud*, *Eddington* and *AAPA*, as applied to claim 13, in further view of *Welch*.

Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud*, *Eddington* and *AAPA*, as applied to claim 13, in further view of *Nakamura*.

Claim 17 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Lavaud*, *Eddington* and *AAPA*, as applied to claim 13, in further view of *Tanikawa*.

B. Discussion of the Rejections

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Accordingly, the prior art must properly disclose, teach or suggest each element of the claimed invention.

1. Claims 1 and 6

Without conceding the propriety of the asserted combination, Applicant's claim 1, as amended, is allowable over the proposed combination of *Lavaud* and *Eddington* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claims.

Specifically, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not apply an output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter.

In contrast with Applicant's claimed IC, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit. Applicant respectfully submits that *Eddington* does not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter."

Accordingly, the combination of *Lavaud* and *Eddington* does not establish a *prima facie* case of obviousness against Applicant's claim 1.

Because independent claim 1 is allowable, dependent claim 6, which depends directly from claim 1, is also allowable. *See In re Fine*, 837, F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Accordingly, Applicant respectfully requests that the rejection of claims 1 and 6 be withdrawn.

2. Claim 2

Without conceding the propriety of the asserted combination, Applicant's claim 2 is allowable over the proposed combination of *Lavaud*, *Eddington* and *Welch* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claim.

Specifically, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC,

the single pin being further coupled to an amplifier subsystem via a filter."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not apply an output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter.

In contrast with Applicant's claimed IC, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit.

Welch is introduced for the teaching of a square-wave generator within a range from 500Hz to 5kHz.

Applicant respectfully submits that *Eddington* and *Welch* do not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter."

Accordingly, the combination of *Lavaud*, *Eddington* and *Welch* does not establish a *prima facie* case of obviousness against Applicant's claim 2.

Therefore, Applicant respectfully requests that the rejection of claim 2 be withdrawn.

3. Claims 3 and 4

Without conceding the propriety of the asserted combination, Applicant's claims 3 and 4 are allowable over the proposed combination of *Lavaud*, *Eddington* and *Nakamura* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claims.

Specifically, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not apply an output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter.

In contrast with Applicant's claimed IC, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit.

Nakamura is introduced for the teaching of a 5-bit counter having a counter frequency on the order of megahertz (MHz).

Applicant respectfully submits that *Eddington* and *Nakamura* do not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter."

Accordingly, the combination of *Lavaud*, *Eddington* and *Nakamura* does not establish a *prima facie* case of obviousness against Applicant's claims 3 and 4.

Therefore, Applicant respectfully requests that the rejection of claims 3 and 4 be withdrawn.

4. Claim 5

Without conceding the propriety of the asserted combination, Applicant's claim 5 is allowable over the proposed combination of *Lavaud*, *Eddington* and *Tanikawa* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claim.

Specifically, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not apply an output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter.

In contrast with Applicant's claimed IC, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit.

Tanikawa is introduced for the teaching of a register that controls a pulse width.

Applicant respectfully submits that *Eddington* and *Tanikawa* do not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter."

Accordingly, the combination of *Lavaud*, *Eddington* and *Tanikawa* does not establish a *prima facie* case of obviousness against Applicant's claim 5.

Therefore, Applicant respectfully requests that the rejection of claim 5 be withdrawn.

5. Claim 8

Without conceding the propriety of the asserted combination, Applicant's claim 8 is allowable over the proposed combination of *Lavaud* and *Welch* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claim.

Specifically, the proposed combination fails to disclose, teach or suggest at least the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem."

The circuit and method disclosed by *Lavaud* does not apply a modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem.

In contrast with Applicant's claimed method, *Lavaud* introduces an OR gate, a microprocessor, which includes a counter, memory and a comparator, as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier. In accordance with column 2, lines 10-14, the signal emitted by the counter is forwarded by a bus line B to a digital-to-analog converter, the analog-output voltage of which is used to control an amplifier. In accordance with column 2, lines 21-23, when an H level is emitted from the comparator, AND gate G1 prevents additional pulses, I, from reaching the counter. Accordingly, the counter state remains steady (i.e., the signal on bus B is constant) and cannot be increased, even when the incremental generator (volume control) is activated.

In contrast with *Lavaud*, which applies a steady-state counter value to the digital-to-analog converter when the comparator output indicates that the volume control threshold has been exceeded, Applicant's claimed method includes the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem." *Lavaud* does not disclose, teach, or suggest Applicant's claimed method step.

Welch is introduced for the teaching of a square-wave generator within a range from 500Hz to 5kHz.

Applicant respectfully submits that *Welch* does not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem."

Accordingly, the combination of *Lavaud* and *Welch* does not establish a *prima facie* case of obviousness against Applicant's claim 8.

Therefore, Applicant respectfully requests that the rejection of claim 8 be withdrawn.

6. Claims 9 and 10

Without conceding the propriety of the asserted combination, Applicant's claims 9 and 10 are allowable over the proposed combination of *Lavaud* and *Nakamura* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claims.

Specifically, the proposed combination fails to disclose, teach or suggest at least the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem."

The circuit and method disclosed by *Lavaud* does not apply a modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem.

In contrast with Applicant's claimed method, *Lavaud* introduces an OR gate, a microprocessor, which includes a counter, memory and a comparator, as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier. In accordance with column 2, lines 10-14, the signal emitted by the counter is forwarded by a bus line B to a digital-to-analog converter, the analog-output voltage of which is used to control an amplifier. In accordance with column 2, lines 21-23, when an H level is emitted from the comparator, AND gate G1 prevents additional pulses, I, from reaching the counter. Accordingly, the counter state remains steady (i.e., the signal on bus B is constant) and cannot be increased, even when the incremental generator (volume control) is activated.

In contrast with *Lavaud*, which applies a steady-state counter value to the digital-to-analog converter when the comparator output indicates that the volume control threshold has been exceeded, Applicant's claimed method includes the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem." *Lavaud* does not disclose, teach, or suggest Applicant's claimed method step.

Nakamura is introduced for the teaching of a 5-bit counter having a counter frequency on the order of megahertz (MHz).

Applicant respectfully submits that *Nakamura* does not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least the step of "applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem."

Accordingly, the combination of *Lavaud* and *Nakamura* does not establish a *prima facie* case of obviousness against Applicant's claims 9 and 10.

Therefore, Applicant respectfully requests that the rejection of claims 9 and 10 be withdrawn.

7. Claims 13 and 18

Without conceding the propriety of the asserted combination, Applicant's claims 13 and 18 are allowable over the proposed combination of *Lavaud*, *Eddington* and *AAPA* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claims.

Specifically, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not connect an amplifier subsystem to an IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal.

In contrast with Applicant's claimed IC, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit.

AAPA is introduced for the teaching of an amplifier subsystem connected to an integrated circuit.

Applicant respectfully submits that *Eddington* and *AAPA* do not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

Accordingly, the combination of *Lavaud*, *Eddington* and *AAPA* does not establish a *prima facie* case of obviousness against Applicant's claims 13 and 18.

Therefore, Applicant respectfully requests that the rejection of claims 13 and 18 be withdrawn.

8. Claim 14

Without conceding the propriety of the asserted combination, Applicant's claim 14 is allowable over the proposed combination of *Lavaud*, *Eddington*, *AAPA* and *Welch* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claim.

Specifically, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not connect an amplifier subsystem to an IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal.

In contrast with Applicant's claimed IC, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit.

AAPA is introduced for the teaching of an amplifier subsystem connected to an integrated circuit.

Welch is introduced for the teaching of a square wave generator having a frequency of 500Hz.

Applicant respectfully submits that *Eddington*, *AAPA* and *Welch* do not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

Accordingly, the combination of *Lavaud*, *Eddington*, *AAPA* and *Welch* does not establish a *prima facie* case of obviousness against Applicant's claim 14.

Therefore, Applicant respectfully requests that the rejection of claim 14 be withdrawn.

9. Claims 15 and 16

Without conceding the propriety of the asserted combination, Applicant's claims 15 and 16 are allowable over the proposed combination of *Lavaud*, *Eddington*, *AAPA* and *Nakamura* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claims.

Specifically, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not connect an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal.

In contrast with Applicant's claimed IC, *Lavaud* introduces an OR gate, a microprocessor (including a counter, a memory and a comparator), as well as a digital-to-

analog converter, all of which further process an audio signal before the audio signal is coupled to an amplifier.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit.

AAPA is introduced for the teaching of an amplifier subsystem connected to an integrated circuit.

Nakamura is introduced for the teaching of a 5-bit counter having a counter frequency on the order of megahertz (MHz).

Applicant respectfully submits that *Eddington*, *AAPA* and *Nakamura* do not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

Accordingly, the combination of *Lavaud*, *Eddington*, *AAPA* and *Nakamura* does not establish a *prima facie* case of obviousness against Applicant's claims 15 and 16.

Therefore, Applicant respectfully requests that the rejection of claims 15 and 16 be withdrawn.

10. Claim 17

Without conceding the propriety of the asserted combination, Applicant's claim 17 is are allowable over the proposed combination of *Lavaud*, *Eddington*, *AAPA* and *Tanikawa* for at least the reason that the combination fails to disclose, teach or suggest each feature in the claim.

Specifically, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

As shown above, *Lavaud* discloses an audio system that applies a constant counter output value when a comparator indicates that a volume control signal has exceeded a threshold value. *Lavaud* does not connect an amplifier subsystem

connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal.

Eddington is introduced for the teaching of placing a plurality of elements on an integrated circuit.

AAPA is introduced for the teaching of an amplifier subsystem connected to an integrated circuit.

Tanikawa is introduced for the teaching of a register that controls a pulse width.

Applicant respectfully submits that *Eddington*, *AAPA* and *Tanikawa* do not add anything to the disclosure of *Lavaud* that would remedy the aforementioned deficiency. That is, the proposed combination fails to disclose, teach or suggest at least "an amplifier subsystem connected to said IC via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal."

Accordingly, the combination of *Lavaud*, *Eddington*, *AAPA* and *Tanikawa* does not establish a *prima facie* case of obviousness against Applicant's claim 17.

Therefore, Applicant respectfully requests that the rejection of claim 17 be withdrawn.

CONCLUSION

Applicant respectfully submits that pending claims 1-11 and 13-18 are allowable and that the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

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